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SPECIAL FEATURE

FPGAs Pave New Processing Paths for VPX and VME Systems

Military applications like radar and military communications have an almost endless appetite for complex signal processing. The latest generation of FPGA offerings married with VME and VPX is feeding those needs.

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Every new FPGA generation delivers more DSP horsepower, higher resource densities, more memory and faster interfaces. Because FPGAs are so well suited to embedded computing boards, these benefits translate directly into higher performance for VME and VPX software radio systems. Specifically, additional DSP48E1 engines, faster DDR3 SDRAM memory interfaces, higher-speed gigabit serial links for Aurora and PCIe, and improved look-up table architectures, all support faster benchmarks and system throughput for FFTs, pattern recognition, target identification and tracking, decoding and decryption, signal analysis and classification, and low-latency countermeasure processing tasks.

The latest board level products for real-time embedded systems have directly benefitted from these new features through new system architectures and interconnection strategies. FPGA resources in the latest Xilinx Series-7 family target various aspects of compute-intensive signal processing for VPX and VME radar and communications applications.

New FPGA Generation

Xilinx's newest generation of FPGAs is the Series 7, based upon low-power 28nm process technology to implement DSP resources of up to 6.7 TMACs, I/O transfer rates of 3.1 Terabits/s, and over 2 million logic cells. Series 7 is split into three families, each addressing different performance/price market spaces: Artix-7, Kintex-7 and Virtex-7.

With a two-fold increase in performance and resources over the previous Virtex-6 devices, the Virtex-7 family targets the highest performance applications often required by Mil/Aero embedded systems. The 28nm Series 7 process technology, coupled with some clever power management techniques, results in a 50 percent reduction in power for a given function. Figure 1 compares the maximum FPGA resources and relative power dissipation levels between the Virtex-6 and Virtex-7 devices. To better address signal processing tasks, the maximum number of DSP blocks has increased by a factor of 2.5. Military embedded systems benefit significantly from this combination of lower power and higher performance for each of the key resources, by opening up new product markets and extending the capabilities of existing applications.

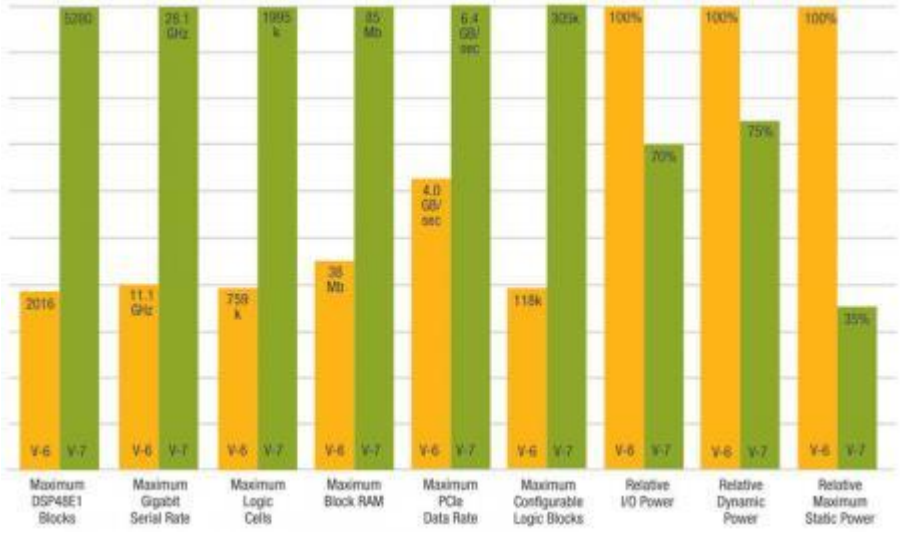

Figure 1
Compared here are the key resources and power consumption of the Virtex-6 and Virtex-7 devices.
Gigabit Serial Links

Traditional parallel buses like VME have become serious bottlenecks because of higher speed peripherals and processors and high-density packaging. Just as desktop PCs have migrated away from PCI and PCI-X toward PCIe (PCI Express), new embedded system architectures like VPX abandon parallel backplane buses in favor of switched serial fabrics and gigabit serial links. The two main advantages are higher speed interconnects and multiple simultaneous paths between software radio system boards and components. More than any other device, FPGAs are the enabling technology for the migration from VME to VPX.

Protocol engines for specific standards can be configured using FPGA logic for different protocols as required. They correctly process protocol-specific packets, header information, control functions, error detection and correction and payload data format. The strategy makes FPGA-based modules

truly “fabric agnostic” and allows one hardware design to be deployed in several different fabric environments.

This flexibility in using one hardware product to cover several different protocols in VPX systems encourages board vendors to develop FPGA-based products for the general market. It also affords system integrators the luxury of not having to commit to any particular standard when selecting boards for their systems. In their latest Virtex-7 devices, Xilinx offers gigabit serial transceivers with four different bit rates: 6.6 GHz (GTP), 12.5 GHz (GTH), 13.1 GHz (GTX) and 28 GHz (GTZ).

Xilinx FPGAs advance gigabit serial technology even further by including integrated PCI interface blocks for PCI Express that incorporate key layers of the PCI Express protocol stack. This saves FPGA resources for other tasks and offers a standardized solution for sending and receiving data using one of the most popular system protocols.

Some Virtex-7 devices now support the PCI Express Base Specification 3.0 with capabilities for both endpoint and root port. Since each generation also accommodates lower generation devices, the Gen3 interface, which operates at 8 Gbits/s, is backward compatible with Gen1 at 2.5 Gbits/s and Gen2 at 5 Gbits/s. The integrated PCIe interface blocks can be configured for 1, 2, 4 or 8 lanes and advanced buffering schemes raise the size to 1024 bytes for maximum sustained throughput rates.

Radar and Wideband Military Comms

Advanced radar systems and new wideband military communications standards like SRW require channel bandwidths of 20 MHz and beyond (Figure 2). To handle these new signals, embedded software radio systems seek to digitize and process signals as close to the antenna as possible. Because these wideband signals implement complex modulation schemes, the parallel processing horsepower of FPGAs is well matched to real-time tasks like encryption and decryption, beamforming and decoding. However, these higher signal bandwidths require faster data converters.

Figure 2
By using JTRS handheld radios, soldiers can make use of wideband waveforms to move voice information further and more efficiently than legacy waveforms across the battlefield through ad-hoc mobile networking.

Monolithic A/D converters suitable for embedded systems have steadily boosted maximum sampling rates. As an example, the National Semiconductor ADC12D1800 3.6 GHz 12-bit A/D converter can now digitize signal bandwidths of 1500 MHz. The digital interface splits the data path into four 12-bit demultiplexed outputs, each operating at 900 MHz. Of course, the problem now becomes how to connect these devices to the necessary signal processing elements. At these high rates, interconnecting traces require controlled impedances, matched lengths and proper termination.

The latest Virtex-7 FPGAs provide a direct connection to these types of high-speed peripheral devices with I/O transfer rates reaching 1866 MHz. They include per-bit skew adjustments to help align bits in a data word, easing the onerous printed circuit board layout constraints of trace length matching. Digitally controlled termination networks eliminate the need for external discrete resistors and aid in tuning the links for optimum performance. Figure 3 shows a 3U OpenVPX Virtex-7 software radio module using the 3.6 GHz A/D converter and taking full advantage of the high-speed I/O capabilities of the FPGA.

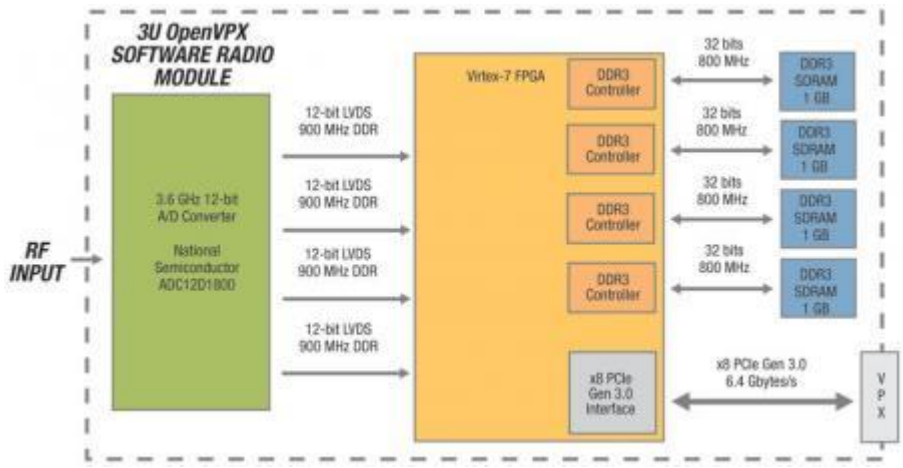

Figure 3
Virtex-7 provides direct interfacing to a 3.6 GHz 12-bit A/D converter through four demultiplexed DDR ports operating at 900 MHz each. Four Gbytes of DDR3 SDRAM can capture, buffer and delay A/D data at the full sample rate. The x8 PCIe Gen 3.0 system interface delivers data at 6.4 Gbytes/s.
Memory Interfaces for VME, VPX

Virtually all VME and VPX embedded systems require deep and fast memory for storage, processing and buffering data. The densest and most economical solution for large memory arrays is the SDRAM. In addition, DDR3 SDRAMs transfer data at both edges of the clock to deliver extremely fast read/write writes. At these speeds, interface timing for each memory must be carefully tuned for reliable operation. For this reason, DDR3 memory controllers must include high-resolution programmable delay elements and training algorithms, so that optimum timing parameters can be calibrated each time the system is powered up.

The latest Virtex-7 devices can support DDR3 devices running bit transfer rates up to 1.866 Gbits/s. Special FPGA I/O pins allow a direct, glueless connection to these memories. To support these extreme speeds, Xilinx developed the Phasor clock generator in the Virtex-7, which allows a 1:4 ratio between the logic fabric clock and the memory clock, doubling the 1:2 ratio for the Virtex-6. Figure 3 shows direct connections from the FPGA to four 1 Gbyte banks of DDR3 SDRAM capable of capturing, buffering and delaying data samples from the 3.6 GHz A/D in real time with no data loss.

Data Buffering

Once high-speed peripherals have been successfully interfaced to the FPGA, the designer must now deal with managing the staggering flow of data to and from other system resources. While A/D and D/A converters operate at a constant clock rate, networks and VPX system buses transfer data in packets or blocks.

Block RAM resources of FPGAs can be used as FIFOs to provide an elastic data buffer for some applications. In other cases, a swinging buffer memory is more appropriate, especially for block-oriented bus interfaces. A swinging buffer, also built from FPGA internal block RAM, allows one memory bank to be filled from one resource (like an A/D converter) while another bank is being emptied by another resource (like the PCIe interface). These schemes are extremely effective when the average data rate of peripheral is less than the average rate of the system interface. The largest Virtex-7 devices now offer more than 10 Mbytes of internal block RAM, more than twice as much as the previous generation.

However, transient capture applications like radar require a large amount of data to be captured at a very high rate in real time during a range gate, even though the duty cycle of the gate is relatively low. In this case, because FPGA block RAM is too small, external memory must be used, and the specialized SDRAM interfaces discussed above come into play. In these applications, duty cycle averaging allows the system interface to operate at a much lower speed with no data loss.

Riding the FPGA Wave

For example, in a radar system, a 3.6 GHz A/D converter VPX module as shown in Figure 3 generates sample data at 4.8 Gbytes/s (assuming 1.5 bytes per sample). For a range gate of 100 msec duration, the capture buffer size must be 480 Mbytes, fitting nicely within any of the four 1 Gbyte SDRAMs. If the duty cycle is 20%, data in the buffer must be delivered to the system interface at an average rate of only 960 Mbytes/s, a reasonable rate for most VPX backplane interconnects.

Virtually every aspect of a VME or VPX module can benefit from this new FPGA technology. Faster gigabit serial links with internal PCIe engines, faster memory controllers, higher-speed peripheral and sensor interfaces, plus greatly enhanced DSP capabilities offer a tremendous performance boost to embedded system applications. This is especially critical for unmanned vehicles, where size, weight and power dominate as key factors. As FPGA vendors continue to compete for design wins by offering new features, better performance, higher density and lower power, VME and VPX designers must constantly track the industry to take best advantage of these powerful components.

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